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(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure
3. X Drawings(s) (35 USC 113) (Total Sheets 6)
4. X Oath or Declaration (Total Pages 3)
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6. Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission

JC377 U.S. PTO

09/458121



12/08/99

Year	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

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NAME John P. Ward Reg No.: 41,216

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

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APPLICATION FOR UNITED STATES LETTERS PATENT

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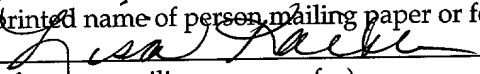
**Method and Apparatus for Stack
Emulation During Binary Translation**

Inventors: Gal Moas
Orna Etzion

Prepared by:
Blakely, Sokoloff, Taylor & Zafman
1279 Oakmead Parkway
Sunnyvale, California 94086
(408) 720-8598

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**Method and Apparatus for Stack
Emulation During Binary Translation**

FIELD OF THE INVENTION

5

The present invention relates to the field of computer emulation. In particular the present invention discloses methods for emulating a computer processor architectural stack.

10 **BACKGROUND OF THE INVENTION**

As new computer processors are designed, new computer architectural designs are created. The new computer architecture designs improve the processing performance of the new computer processors. However, 15 the existing set of computer programs often can not directly execute on new computer architectures.

To run computer object code written for an older computer architecture on a newer computer processor, many computer systems use 20 software that will "emulate" the older computer processor architecture. Specifically, software running on the newer computer processors simulates the actions of the older computer processor by interpreting each instruction. Software emulators work well for executing many legacy applications. However, software emulation wastes processor power due to the emulation 25 software overhead.

Another method of running computer object code written for an older computer architecture on a new computer processor is to perform binary translation. A binary translator translates blocks of code written for an older source architecture into equivalent blocks of code in the newer target processor architecture. The translation can be done "on the fly" (while "executing" the older source architecture code). Translation could also be done before execution. By translating the old source architecture code into code for the newer processor architecture, the overhead of the emulation code is eliminated. Thus, binary translation often provides better performance than emulation.

When executing older code, both software emulation systems and binary translators must precisely duplicate the environment of the older processor architecture. Software emulators duplicate the behavior of the older processor architecture by providing an interpreter that interprets each microprocessor instruction as the original processor would have. Binary translators provide a duplicate environment by inserting extra instructions as necessary to ensure that various parameter limits of the older processor are not being exceeded. Since the extra instructions are not directly related to the goal of the original program, these extra instructions are "overhead" code that reduce performance. It would be desirable to implement binary translators in a manner that minimizes the amount of overhead code that needs to be added to duplicate the environment of the older processor architecture.

SUMMARY OF THE INVENTION

A method and apparatus for monitoring processor resources is disclosed. To monitor a processor resource, first a set of needed resources is
5 determined at the beginning of a block of code. A test is then performed to determine if the set of needed resources is available at the start of the block of code. An error is signaled if the needed resources are not available at the beginning of the block of code.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A conceptually illustrates one possible initial state of a processor stack.

5 **Figure 1B** conceptually illustrates the state of a processor stack after starting from the initial processor stack state of **Figure 1A** and executing the first instruction of code listing 1.

10 **Figure 1C** conceptually illustrates the state of a processor stack after starting from the processor stack state of **Figure 1B** and executing the second instruction of code listing 1.

15 **Figure 1D** conceptually illustrates the state of a processor stack after starting from the processor stack state of **Figure 1C** and executing the third instruction of code listing 1.

Figure 2 is a flow diagram describing the steps of monitoring the processor resources according to one embodiment.

20 **Figure 3** illustrates a computer system having a computer readable medium with instructions stored thereon according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A method and apparatus for emulating a computer processor architectural stack is disclosed. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. For example, the present invention has been described with reference to the Intel architecture floating point stack. However, the same techniques can easily be applied to other types of stacks in other computer processors.

As previously set forth, legacy applications that were written for an older processor architecture can be run on a new processor architecture by using an emulator or a binary translator. With either solution, a significant amount of "overhead" code must be added to have the new processor architecture simulate the actions of the older processor architecture.

Processor exceptions are one specific aspect of an older processor architecture that must be duplicated. If a resource limit of the older processor architecture is exceeded in a manner that would cause an exception, for example a stack over flows, then an appropriate processor exception is to be generated. In order to generate exceptions at appropriate times, the overhead code keeps track of processor resources to monitor whether the older processor architecture limits have not been exceeded.

To illustrate how prior art software emulators and binary translator systems handle exceptions, an example is provided. The following example illustrates the traditional approach for validating stack limitations. The following code lists a short program for 32-bit Intel architecture processors.

Code Listing 1: Example Source Processor Code

```
FLD <mem>          ;Push a value onto the floating point stack
FSTP <dest1>        ;Pop a value off of the floating point stack
FSTP <dest2>        ;Pop a value off of the floating point stack
```

The first line of the 32-bit Intel architecture pushes a floating point value from a memory location <mem> onto the processor's floating point stack. The second line of code pops a value off the processor's floating point stack and puts the value into a destination memory location <dest1>. The third line of code pops a value off the processor's floating point stack and puts the value into a destination memory location <dest2>.

Figures 1A to 1D conceptually illustrate how the above example would cause an exception when run in a processor that has an empty stack.

Figure 1A conceptually illustrates an initial state with an empty floating point stack. Figure 1B conceptually illustrates how the floating point stack appears after the FLD <mem> instruction executes and places a value onto the floating point stack. Figure 1C conceptually illustrates how the floating point stack appears after the FSTP <dest1> instruction executes and pops the value off the floating point stack. Finally, Figure 1D conceptually illustrates why the final instruction conceptually illustrates why the instruction FSTP <dest2> causes an exception when it executes. Specifically, an underflow exception occurs since the

FSTP <dest2> instruction attempts to pop a value off an empty floating point stack.

To detect such stack underflows, prior art systems typically add overhead code that keeps track of the floating point stack state. At each instruction that affects the floating point stack, the overhead code checks to ensure that no overflow or underflow has occurred. Specifically, the binary translator creates a stack check sequence for each stack operation. The following example code presents code that might be created by a prior art binary translator:

Code Listing 2: Prior Art Binary Translator code:

```
ADD top = top - 1           ;decrement stack top (Push)
CMP stack[top] == empty    ;validate stack top to be empty
BRNE FaultHandler         ;Else - go to fault handler function
FLD stack[top] = <mem>     ;Load to stack top
```

```
CMP stack[top] == non empty ;validate stack top to be non empty
BRNE FaultHandler         ;Else - go to fault handler function
FLD <dest1> = stack[top]   ;store from stack top
ADD top = top + 1         ;Increment stack top (pop)
```

```
CMP stack[top] == non empty ;validate stack top to be non empty
BRNE FaultHandler         ;Else - go to fault handler function
FLD <dest2> = stack[top]   ;store from stack top
ADD top = top + 1         ;Increment stack top (pop)
```

In the prior art binary translator code, a "top" variable maintains a stack top pointer and a "stack" array maintains the contents of the stack. The first four lines simulate the FLD <mem> instruction of the original code. Two instructions (the Compare "CMP" and Branch If Not Equal "BRNE" instructions) ensure that the stack contains an empty position before the push onto the floating point stack

occurs. If the stack pointer does not point to an empty stack position, then the program will branch to a fault handler routine labeled "FaultHandler".

5 The next four lines of the prior art binary translator code simulate the first "FSTP" instruction that pops a value off the floating point stack and stores that value into a defined location. The code first ensures that the floating-point stack position at the top of the stack is not empty. After this has been verified, the pop is emulated by storing the value at the top of the floating-point stack into the defined <dest1> memory location. Similarly, the last four lines of
10 code simulate the final "FSTP" instruction that pops a value off the floating point stack and stores that value into a defined location.

As illustrated above, the overhead code that keeps track of resources can significantly enlarge the original code. In the above example, the
15 original three lines of code expanded into twelve lines of code. The extra instructions can significantly degrade the software performance.

Improved Resource Monitoring for Emulation and Binary Translation

20 To improve the performance of emulators and binary translators, the present invention introduces an improved method of Monitoring processor resources. In one embodiment, a short set of instructions at the beginning of a block of code checks to determine if needed processor resources are available at the beginning of a block of code. If the needed resources are available, then

execution proceeds. The code then modifies the set of available resources according to the resource requirements of the instructions in the block of code.

By performing a check at the start of a block of code rather than at each instruction addressing the stack, the system of the present invention can provide a significant performance advantage. The check is performed in the block header and thus saves cycles and code size. Furthermore, numerous branches to the fault handling function are removed. Removing branch instructions can significantly improve performance since mispredicted branches may cause processor stalls. Finally, the improved code is easier to schedule.

In one embodiment of the present invention, a register is used to keep track of the stack contents. Specifically, in one embodiment, a set of bits in a designated register are associated with the available stack entries. If a particular bit is clear then the associated stack entry is empty. Similarly, if a particular bit is set then the associated stack entry is non-empty. To verify that the stack contains the needed resources, a needed stack state is compared with the current stack state representation. If the current stack state does not match the needed stack state then a processor exception may be generated.

To illustrate the teachings of the present invention, an example is hereby provided with reference to the previous provided sample code of Code Listing 1. The following example code uses an array named "stack" that contains the contents of the simulated floating-point stack. The example code uses a "top" variable as a stack pointer into the "stack" array. Finally, the example uses

a binary status representation of stack entries known as the <stack register> that contains the status (non-empty or empty) of each stack entry. Specifically, in one embodiment, a set bit in the <stack register> indicates an associated non-empty stack entry and a clear bit indicates an associated empty stack entry. Note that

5 the following example assumes that the stack pointer is pointing to the top of the stack (the leftmost position in the stack status register). In alternative embodiments, the stack pointer may point to the right most position.

Code Listing 3: Improved Translated Code

```

10 ; Check sequence that tests the stack
    AND <tmp register> = <stack register>, <11000...0>
        ;Extract the relevant stack bits (in the example - the first 2 bits)
    CMP <tmp register> == <10000..0>
        ;Compare to needed stack (1st entry non empty, 2nd entry empty)
    BRNE FaultHandler          ;Else - go to fault handler function

15 ;Actual code emulation
    ADD top = top - 1           Decrement stack top (push)
    FLD stack[top] = <mem>      Load to stack top
    FLD <dest1> = stack[top]     Store to <dest1> from stack top
    ADD top = top + 1           Increment stack top (pop)
    FLD <dest2> = stack[top]     Store to <dest2> from stack top
    ADD top = top + 1           Increment stack top (pop)
    ;Update the stack register
    XOR <stack register> = <10000..0>, <stack register>
25 ;Reset mask (clear first bit).

```

The example code has been divided into three sections: a check sequence, an emulation sequence, and an update sequence. The check sequence determines if the required resources are available. The emulation code sequence performs the

30 intended operation of the source code. The update sequence updates the resource Monitoring variables.

Figure 2 is a flow diagram describing the steps of monitoring processor resources as set forth in the code listing 3. In processing block 202, the first instruction (the "AND" instruction) logically ANDs the stack register with a value that specifies the relevant bits. In the example source code (code listing 1), one push and two pops are performed. Thus, the two positions a near the top of the stack should be examined. The AND operation reflects this by masking off all bits of the stack status register except for the first two bits (the two entries associated with the top of the stack) and placing the result in a temporary register.

In processing block 204, a compare ("CMP") operation compares the temporary register value with the needed stack values. Since a push followed by two pops will be performed, the stack needs an empty position just "above" the top of the stack and a non-empty entry at the top of the stack (to fulfill the second pop). This is represented by the bit vector <10000 ...0> where the first set bit is the non empty position at the top of the stack. The adjacent clear bit is the empty position just above the top of the stack. Note that the other positions are set to zero such that the comparison is not affected by these positions that were masked off from the stack status register value. In alternative embodiments, the bit vector in the temporary register could bit positions cleared rather than set to indicate a non empty position without departing from the present invention.

In processing block 206, if the comparison does not detect a match, then the branch-if-not-equal ("BRNE") instruction will branch to a fault handler

routine. The fault handler routine handles the lack of required resources appropriately. In one embodiment, the fault handler routine simulates an appropriate processor exception. For example, a stack overflow exception may be simulated.

5

After the check sequence has indicated that the needed stack resources are available, in processing block 208 the emulation code begins. The emulation code simulates the push, pop, and pop by using a "top" variable that contains a stack top pointer and a "stack" array that contains the contents of the stack.

10

After the emulation code, in processing block 210 an update code sequence updates the resource Monitoring variables. In this example, an exclusive-OR ("XOR") instruction updates the stack status register by performing an XOR operation with mask that has a 1 set for every stack location whose status has changed.

15

As illustrated in the example code of code listing 3, bit vector constants may be used when the value of the stack pointer is known. However, the system can be generalized in order to handle dynamic situations. To generalize the resource testing system, a method for generating the mask bit vector, the need comparison bit vector and the update bit vector is described. The bit vector creation method examines the code block that needs bit vectors and generates a MASK bit vector for masking off irrelevant bits and a NEEDED bit vector defining a needed state for comparison against the current stack state.

20

25

The bit vector creation method operates by creating two intermediate arrays. The first array is the 'EXPECTED mask', representing the expected stack status when entering a code block. The second array is the
5 'CURRENT mask', representing the current state of the stack as the method proceeds through the code block. Each array contains an entry for each stack location. Each stack location entry can be of type EMPTY, VALID, or UNKNOWN. The following psuedocode provides one method of dynamically generating the bit vectors for resource Monitoring.

Code Listing 4: The Mask Creation code

Initialize all CURRENT array entries to UNKNOWN.
Initialize all EXPECTED array entries to UNKNOWN.

```
5  For each instruction in code block:
    {
        if the instruction is a Read stack entry X then
            {
10         if CURRENT(X) != VALID then
                {
                    EXPECTED(X) = VALID
                    CURRENT(X) = VALID
                }
            }
15         if the instruction is a Push (write) to stack entry X then
            {
                if CURRENT(X) != EMPTY then
20                 {
                    EXPECTED(X) = EMPTY
                }
                CURRENT(X) = VALID
            }
25         if the instruction is a Free (as a part of a pop) stack entry X then
            {
                if CURRENT(X) == VALID then
30                 CURRENT(X) = EMPTY
                else if CURRENT(X) == UNKNOWN then
                    {
                        CURRENT(X) = EMPTY
                        EXPECTED(X) = VALID
35                     }
            }
    }

Initialize all NEEDED bit vector bits to ZERO.
Initialize all UPDATE bit vectors bits to ZERO
40 Initialize all MASK bit vector bits to one
For each entry N in stack:
    {
```

```

        if EXPECTED(N)==VALID then NEEDED(N)=one
        if EXPECTED(N) ==UNKOWN then MASK(N) = zero
        if EXPECTED(N)!= CURRENT(N) then UPDATE(N) = one
    }

```

- 5 It should be noted that the pseudo code of code listing 4 has been generalized for a stack structure that allows stack operations other than just push and pop.

As set forth in code listing four, an EXPECTED array is generated by setting entries that are initially written to as EMPTY and entries that are initially read from as VALID. The NEEDED bit vector is generated by placing a one in for each VALID entry in the EXPECTED array, all other bits are set to zero. The MASK bit vector is generated by setting each bit having an EMPTY or VALID state in the CURRENT array. The UPDATE bit vector is generated by setting each bit where the CURRENT array does not equal the EXPECTED array.

15 The foregoing has described a method and apparatus for monitoring a computer processor architectural stack. It is contemplated that changes and modifications may be made by one of ordinary skill in the art, to the materials, arrangements, and code listings of the present invention without departing from the scope of the invention. For example, throughout the description where bit vectors have been described as having selected bit positions set or clear, in alternative embodiments, whether a selected bit position is set or clear, could be reversed without departing from the scope of the invention.

25 In addition, the methods as described above, including the methods of monitoring the processor resources, can be stored in memory of a computer

system as a set of instructions to be executed. In addition, the instructions to perform the methods as described above could alternatively be stored on other forms of computer-readable medium, including magnetic and optical disks. For example, method of the present invention can be stored on computer-readable
5 mediums, such as magnetic disks or optical disks, that are accessible via a disk drive (or computer-readable medium drive), such as the disk drive shown in Figure 3.

Alternatively, the logic to perform the methods as discussed above,
10 including the methods of monitoring the processor resources, could be implemented in discrete hardware components such as large-scale integrated circuits (LSI's), application-specific integrated circuits (ASIC's) or in firmware such as electrically erasable programmable read-only memory (EEPROM's). Furthermore, in one embodiment, the methods as described above, including the
15 methods of monitoring the processor resources, are included as instructions and/or logic of an processor architecture emulator or binary translator.

Moreover, the methods as described above, including the methods of monitoring the processor resources, in one embodiment, could be performed
20 when compiling source code in prior to executing the source code. Alternatively, the methods could also be performed dynamically as the source code is being executed.

CLAIMS

We claim:

1 1. A method of monitoring processor resources, said method
2 comprising:
3 determining a set of needed resources for a block of code;
4 testing if said set of resources are available at a start of said block of code;
5 and
6 signaling an error if said set of resources needed for said block of code are
7 not available.

1 2. The method as claimed in claim 1, said method further
2 comprising:
3 determining a set of available resources that will be available after said
4 block of code has executed.

1 3. The method as claimed in claim 1 wherein said needed
2 resources comprise stack contents .

1 4. The method as claimed in claim 1 wherein said set of needed
2 resources is determined at a compile time.

1 5. The method as claimed in claim 1 wherein said set of needed
2 resources is determined dynamically.

1 6. The method as claimed in claim 1 wherein signaling said
2 error if said set of resources needed for said block of code are not available
3 comprises branching to a fault handler routine.

1 7. The method as claimed in claim 6 wherein signaling said
2 fault handler routine simulates a processor exception.

1 8. The method as claimed in claim 1 wherein needed resources
2 are represented by a bit vector.

1 9. The method as claimed in claim 8 wherein said bit vector is
2 generated dynamically.

1 10. A computer-readable medium having stored thereon a set of
2 instructions to monitor processor resources, said set of instruction, which when
3 executed by a processor, cause said processor to perform a method comprising:
4 determining a set of needed resources for a block of code;
5 testing if said set of resources are available at a start of said block of code;
6 and
7 signaling an error if said set of resources needed for said block of code are
8 not available.

1 11. The computer-readable medium as claimed in claim 10,
2 wherein said set of instructions further includes additional instructions, which
3 when executed by said processor, cause said processor to perform said method
4 further comprising:
5 determining a set of available resources that will be available after said
6 block of code has executed.

1 12. The computer-readable medium as claimed in claim 10
2 wherein said needed resources comprise stack contents .

1 13. The computer-readable medium as claimed in claim 10
2 wherein said set of needed resources is determined at a compile time.

1 14. The computer-readable medium as claimed in claim 10
2 wherein said set of needed resources is determined dynamically.

1 15. The computer-readable medium as claimed in claim 10
2 wherein signaling said error if said set of resources needed for said block of code
3 are not available comprises branching to a fault handler routine.

1 16. The computer-readable medium as claimed in claim 15
2 wherein signaling said fault handler routine simulates a processor exception.

1 17. The computer-readable medium as claimed in claim 10
2 wherein needed resources are represented by a bit vector.

1 18. The computer-readable medium as claimed in claim 17 wherein
2 said bit vector is generated dynamically.

1 19. A computer-readable medium, having stored thereon a first
2 set of instructions, the first set of instructions, which when executed by a
3 processor, generate a second set of instructions through a binary translation
4 process, the second set of instructions when executed by the processor, cause
5 said processor to perform a method comprising:
6 determining a set of needed resources for a block of code;
7 testing if said set of resources are available at a start of said block of code;
8 and
9 signaling an error if said set of resources needed for said block of code are
10 not available.

1 20. The computer-readable medium as claimed in claim 19,
2 wherein said set of instructions further includes additional instructions, which
3 when executed by said processor, cause said processor to perform said method
4 further comprising:
5 determining a set of available resources that will be available after said
6 block of code has executed.

1 21. The computer-readable medium as claimed in claim 19
2 wherein said needed resources comprise stack contents .

1 22. The computer-readable medium as claimed in claim 19
2 wherein said set of needed resources is determined dynamically.

1 23. The computer-readable medium as claimed in claim 19
2 wherein signaling said error if said set of resources needed for said block of code
3 are not available comprises branching to a fault handler routine.

1 24. The computer-readable medium as claimed in claim 23
2 wherein signaling said fault handler routine simulates a processor exception.

1 25. The computer-readable medium as claimed in claim 19
2 wherein needed resources are represented by a bit vector.

ABSTRACT OF THE DISCLOSURE

A method of monitoring processor resources. To monitor a processor resource, first a set of needed resources is determined at the beginning of a block of code. A test is then performed to determine if the set of needed
5 resources is available at the start of the block of code. An error is signaled if the needed resources are not available at the beginning of the block of code.

663027-23460

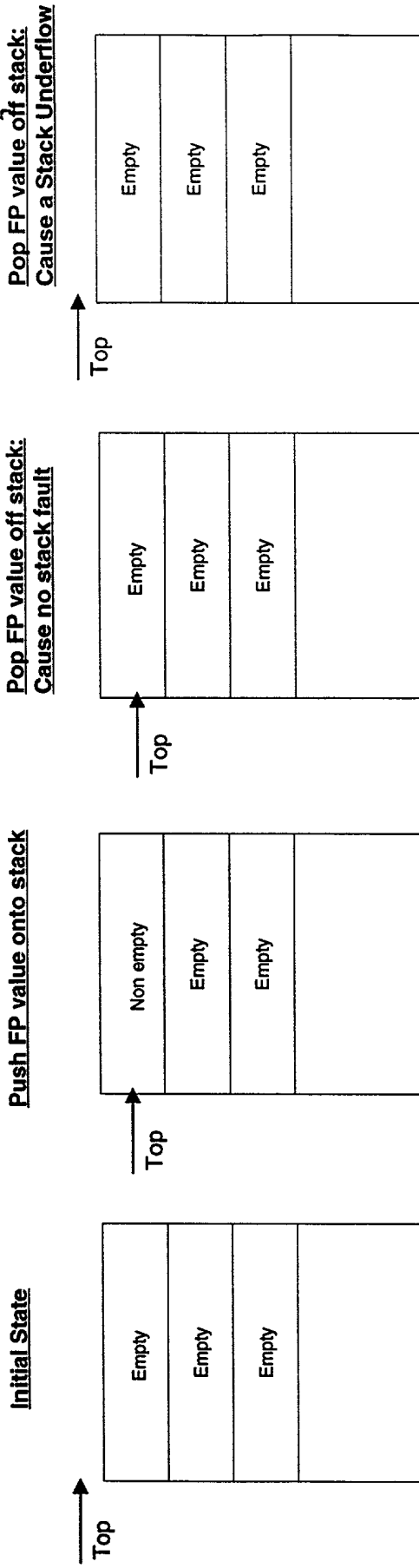


Figure 1A

Figure 1B

Figure 1C

Figure 1D

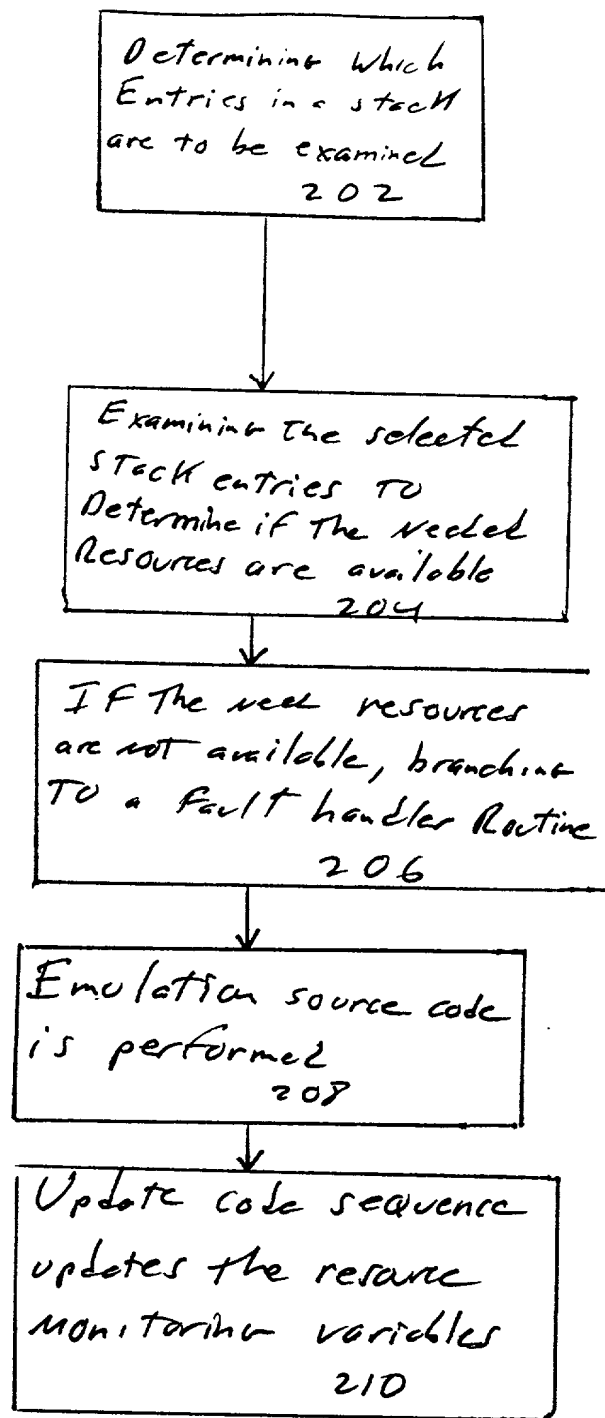


Fig. 2

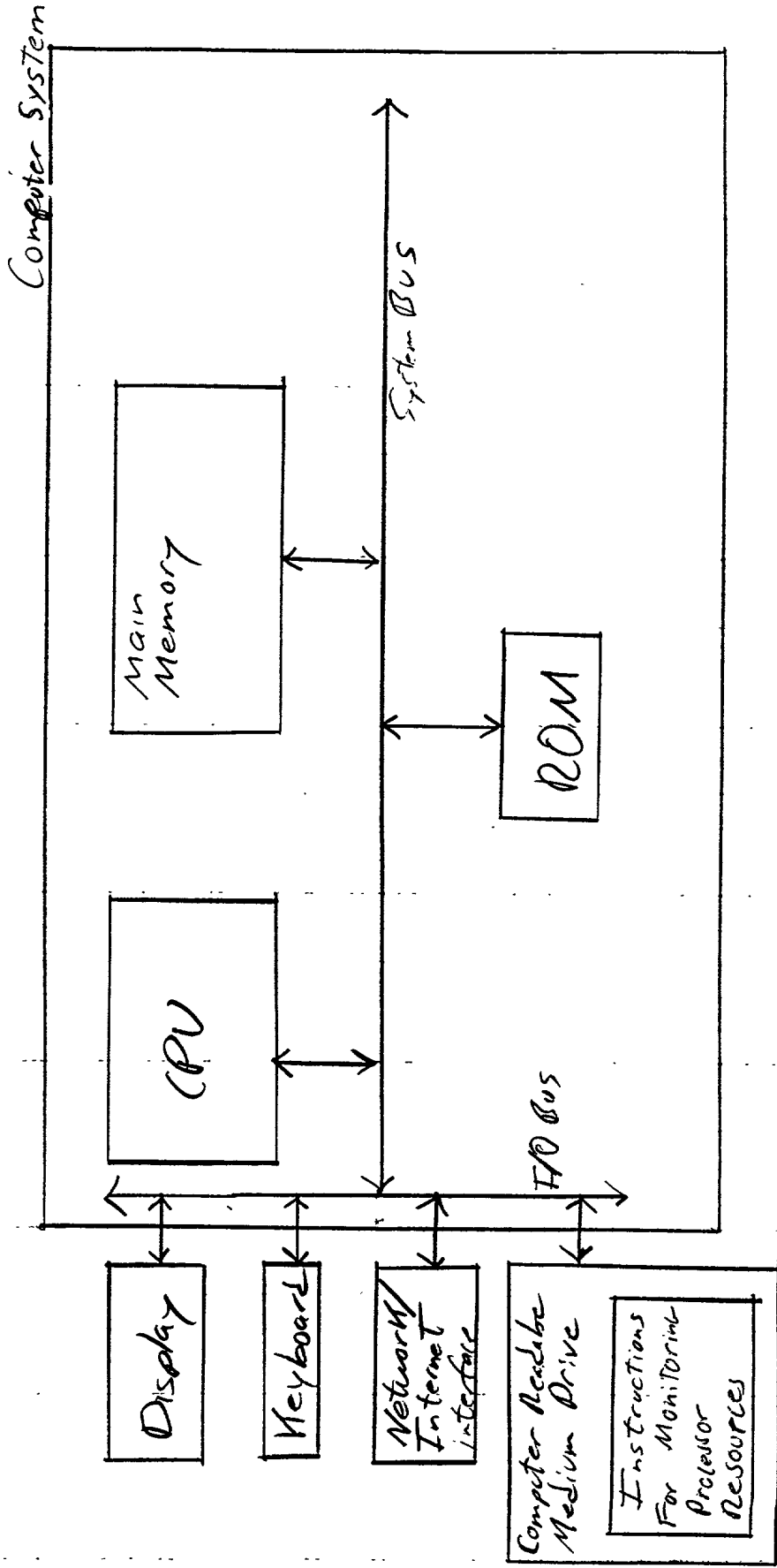


Fig. 3

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method And Apparatus For Stack Emulation During Binary Translation.

the specification of which

X is attached hereto.
____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

Priority
Claimed

<u>(Number)</u>	<u>(Country)</u>	<u>(Day/Month/Year Filed)</u>	<u>Yes</u>	<u>No</u>
<u>(Number)</u>	<u>(Country)</u>	<u>(Day/Month/Year Filed)</u>	<u>Yes</u>	<u>No</u>
<u>(Number)</u>	<u>(Country)</u>	<u>(Day/Month/Year Filed)</u>	<u>Yes</u>	<u>No</u>

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

<u>Application Number</u>	<u>Filing Date</u>
<u>Application Number</u>	<u>Filing Date</u>

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

<u>Application Number</u>	<u>Filing Date</u>	<u>Status -- patented, pending, abandoned</u>
<u>Application Number</u>	<u>Filing Date</u>	<u>Status -- patented, pending, abandoned</u>

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to John P. Ward, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct
telephone calls to John P. Ward, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Gal Moal

Inventor's Signature _____ Date _____

Residence K. Byalik, Israel Citizenship Israel
(City, State) (Country)

Post Office Address 5 Ha Dkalim Street
K. Byalik, Israel

Full Name of Second/Joint Inventor Orna Etzion

Inventor's Signature _____ Date _____

Residence Haifa, Israel Citizenship Israel
(City, State) (Country)

Post Office Address 5 Kariv Street
Haifa, Israel

APPENDIX A

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. P44,587; Thomas M. Coester, Reg. No. 39,637; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. No. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaaf, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg. No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells, Reg. No. P43,256; Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56

Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

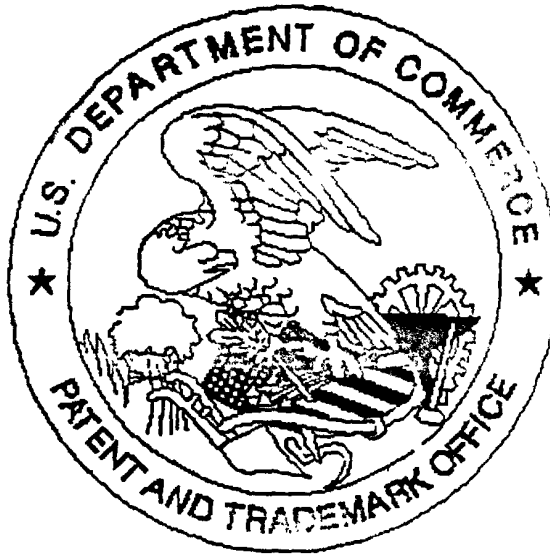
(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

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Application deficiencies were found during scanning:

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*There are 3 sheets of Drawings Enclosed!
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